A Two-Stage Isolated/Bidirectional DC/DC Converter With Current Ripple Reduction Technique

Jun-Young Lee, Yu-Seok Jeong, and Byung-Moon Han

***Abstract*—This letter suggests a two-stage isolated/bidirectional dc/dc converter with three bridges. Two bridges are used for electrical isolation and constant gain, and the bidirectional control is accomplished through only a single bridge. RMS currents in the high-voltage source and link capacitor can be alleviated by capacitor division and synchronizing operation of both stages. This structure provides a simple control scheme and removes snubber circuitry, so a high efficiency can be obtained under a high switching frequency regardless of operational modes.**

***Index Terms*—Bidirectional converter, dc/dc converter, fuel cell.**

I. Introduction

Fuel cell has a slow dynamic response, so the power supply from the fuel cell cannot cope with the power demand during a transient load. Thus, a secondary power source is required to compensate the power difference between the fuel cell and the load, and a battery is generally used to supply a transient power [1]–[4]. The power flow between the fuel cell and the battery is managed by a bidirectional dc/dc converter. Conventional isolated/bidirectional dc/dc converters for high-power applications have a voltage-fed full-bridge (FB) (VF-FB) scheme in the high-voltage (HV) side and various current-fed (CF) schemes in the low-voltage (LV) side in general because voltage-fed half-bridge (HB) and voltage-fed push–pull (PP) schemes have disadvantages of high current stress and/or high voltage stress [5]. According to which schemes are used in the LV side, they have several variations such as VF-FB + two-inductor CF-HB, VF-FB + CF-FB, and VF-FB + CF-PP with six or eight switches. These converters suffer from efficiency decrease at a light-load condition and low efficiency at boost-mode operation due to switching loss [6]. Also, they require a snubber circuit such as an active-clamp circuit to alleviate turn-off voltage spikes in the LV side, which increases the switch number by one or two as a result [7]–[10].

In this letter, a two-stage isolated/bidirectional dc/dc converter adopting a current ripple reduction technique is proposed. The resonant converter with two bridges takes in charge of electrical isolation and constant gain, and the bidirectional control is accomplished using only the second stage with a single bridge. To reduce rms currents in the HV source and link capacitor, capacitor division and synchronizing operation of two stages are adopted. A 2-kW prototype converter has been designed and verified based on design guidelines that are derived from the circuit analysis.

II. Proposed Converter

A. Description of the Proposed Converter

Figs. 1 and 2 show the proposed converter with key waveforms, and its operational mode diagrams are shown in Fig. 3. The resonant converter with a fixed frequency automatically forms bidirectional power flow according to input/output conditions, and the bidirectional control is accomplished using only M_5 and M_6. The bulk capacitors

Manuscript received October 6, 2010; revised December 5, 2010; accepted January 6, 2011. Date of publication January 28, 2011; date of current version October 4, 2011. This work was supported by the National Research Foundation of Korea Grant funded by the Korean Government (MEST) (NRF-2010-R1A5A003-2010-0026283).

The authors are with the Department of Electronics Engineering, Myongji University, Yongin 449-728, Korea (e-mail: pdpljy@mju.ac.kr; jeong@mju.ac.kr; erichan@mju.ac.kr).

Digital Object Identifier 10.1109/TIE.2011.2109343

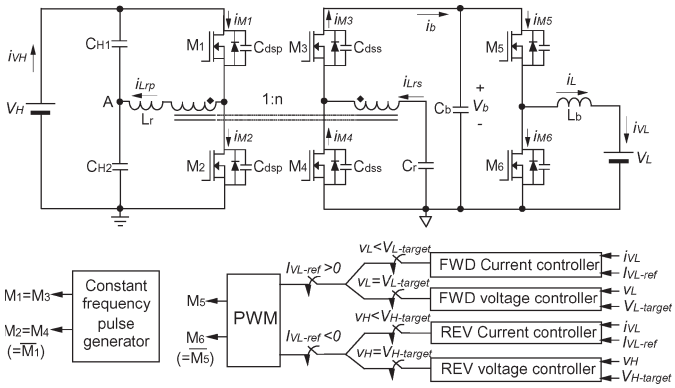

Fig. 1. Schematic of the proposed bidirectional converter.

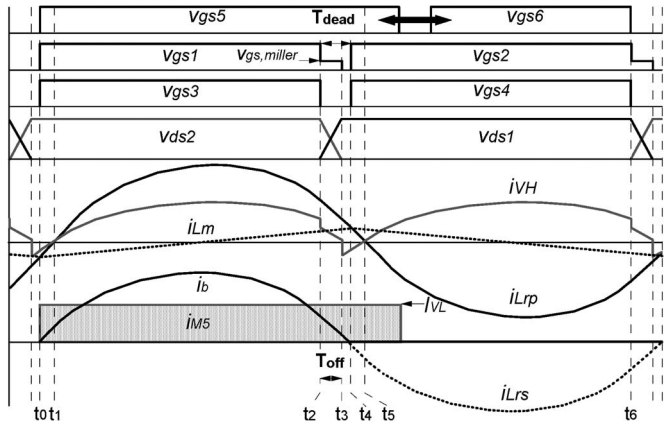

Fig. 2. Operational waveforms of the proposed converter.

C_{H1} and C_{H2} provide resonant current paths to alleviate the current ripple from the HV source. The voltage-doubler structure in the LV side reduces the rms current of the link capacitor C_b by compensating the discharge current, which helps to reduce the link capacitor size. Before explanation, C_{H1} and C_{H2} have the same value, and the resonant frequency f_r is equal to the switching frequency f_s. Also, the second stage is modeled by a pulse current source with the switching frequency synchronized with that of the first stage. Because the resonant converter has a symmetric structure, buck and boost modes have identical operation, and we will explain the operation only with buck mode. When M_1 and M_3 are turned on at t_0, M_1 has zero-voltage switching (ZVS), and the secondary resonant current $i_{\rm Lrs}$ begins to flow through the channel of M_3, the link capacitor C_b, and the resonant capacitor C_r. After the primary resonant current $i_{\rm Lrp}$ crosses zero at t_1, it flows through the channel of M_1 and the resonant inductor L_r. Because the impedances seen from node A to C_{H1} and C_{H2} are identical, $i_{\rm Lrp}$ is divided into half, and each half current flows through the two capacitors. When $v_{\rm gs1}$ is decreased to the Miller plateau voltage $V_{\rm gs,Miller}$ at t_2, the drain–source voltage of $M_1 v_{\rm ds1}$ is linearly increased, and $i_{\rm Lrs}$ flows through the body diode of M_3. The discharge current of the drain–source capacitance of $M_2 C_{\rm dsp}$ can be written as $i_{M2} = -C_{\rm dsp} V_H / T_{\rm off}$, where $T_{\rm off}$ is the turn-off time of M_1. Thus, the HV-side current $i_{\rm VH}$ becomes $i_{\rm Lrp}/2 - C_{\rm dsp} V_H / T_{\rm off}$. After M_1 is completely turned off at t_3, $i_{\rm Lrp}$ starts to flow through the body diode of M_2, and the ON state of the body diode of M_3 is maintained to provide the current path of $i_{\rm Lrs}$. When M_2 and M_4 are turned on at t_4, ZVS of M_2 is accomplished, and $i_{\rm Lrs}$ flows through the channel of M_4 and C_r. After t_5, $i_{\rm Lrp}$ changes its direction, flowing through C_{H1} and C_{H2} similar to mode 2. Thus, $i_{\rm VH}$ also has $i_{\rm Lrp}/2$. Referring to the key waveforms, the current ripple in the HV source is like that of the FB structure, and the charge and discharge currents of C_b happen at the same time. The current cancellation helps to reduce

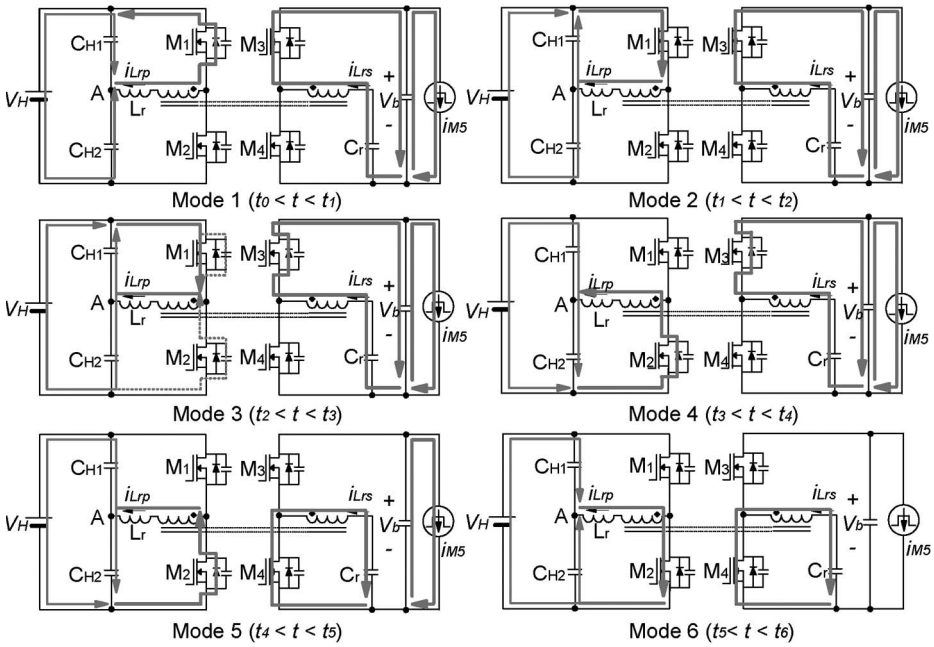

Fig. 3. Operational mode diagrams.

TABLE I
STRUCTURAL COMPARISONS BETWEEN THE PROPOSED CONVERTER AND CONVENTIONAL CONVERTERS

	Conventional converters						
HV side	VF-FB			VF-HB			Proposed converter
LV side	CF-HB	CF-FB	CF-PP	CF-HB	CF-FB	CF-PP	
Switch (With active clamp circuit)	6 (8)	8 (9)	6 (8)	4 (6)	6 (7)	4 (6)	6 (6)
Capacitor	1	1	1	1	1	1	2
Inductor	2	1	1	2	1	1	1

the rms current of C_b that suffers from the heavy current stress. In steady state, the average discharge current of C_b, which is equal to the average LV-side current $I_{\rm VL}$, is balanced with the average charge current so that $i_{\rm Lrs}$ can be written as $i_{\rm Lrs} = \pi D I_{\rm VL} \sin(2\pi f_r t)$, where D is the duty ratio of M_5. Because the magnetizing current $i_{\rm Lm}$ is circulated in the primary side, the effective current supplied from the HV source is equal to half the rectified current $i_{\rm Lrs}$ reflected to the primary side, i.e., $i_{\rm VH} = |n\pi D I_{\rm VL} \sin(2\pi f_r t)/2|$. By averaging this equation, the current gain becomes $I_{\rm VH} = nDI_{\rm VL}$, and it follows that the voltage gain is derived as $V_L = nDV_H$. Thus, the bidirectional power flow is controlled only with D.

B. Structural Comparisons Between the Proposed Converter and Conventional Converters

Table I shows the structural comparisons between the proposed converter and conventional bidirectional converters. The switch block of the proposed converter has a number of advantages over those of basic conventional converters. Considering additional active-clamp circuits to absorb the voltage spikes in conventional converters, the proposed converter has an advantage in the switch block because it does not require any snubber circuitry. The number of magnetic elements in the proposed converter is equal to or less than those of conventional converters. However, the proposed converter has drawbacks in capacitor blocks and diode blocks due to the cascaded structure of two converters. Synthesizing the comparisons, the structure of the proposed converter is not inferior to the conventional converters despite the two-stage structure.

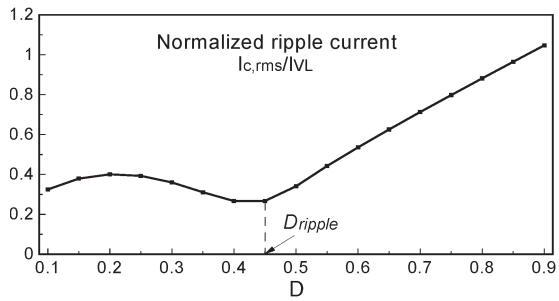

Fig. 4. Normalized ripple current of C_b.

III. DESIGN GUIDELINES

To accomplish the ZVS condition, the peak magnetizing current should be large enough to discharge the drain–source capacitances of MOSFETs during dead time $T_{\rm dead}$. From this condition, the primary magnetizing inductance L_m to meet ZVS both buck and boost modes can be driven as

$$\text{buck mode}: \quad L_{\rm mF} \le T_{\rm sL} T_{\rm dead}/16 C_{\rm dsp} \tag{1}$$

$$\text{boost mode}: \quad L_{\rm mR} \le T_{\rm sL} T_{\rm dead}/16 n^2 C_{\rm dss}. \tag{2}$$

Thus, L_m can be selected as

$$L_m = \min(L_{\rm mF}, L_{\rm mR}) \tag{3}$$

where $C_{\rm dss}$ is the drain–source capacitance of M_3, M_4. In this inequality, the first term is the maximum L_m for ZVS in buck mode, and the second term is that in boost mode. With the expression of $i_{\rm Lrs}$ and the operational waveforms, the rms current of C_b, $I_{c,\rm rms}$, can be calculated as

$$\frac{I_{c,\rm rms}}{I_{\rm VL}} = \begin{cases} \sqrt{(0.5\pi D)^2 + D\cos(2\pi D)}, & D \le 0.5 \\ \sqrt{(0.5\pi D)^2 - D}, & D > 0.5. \end{cases} \tag{4}$$

Using (1), the normalized rms current is shown in Fig. 4, and the minimum value can be obtained at $D_{\rm ripple} = 0.45$. Thus, n can be calculated with $I_{\rm VH,max}/D_{\rm ripple} I_{\rm VL,max}$. $V_{b,\rm min}$ should be larger than $V_{L,\rm max}$ for buck-mode control. In boost-mode control, the second stage should be able to boost $V_{L,\rm min}$ to $V_{b,\rm max}$, but the maximum voltage gain k between them is not recommended higher than five that

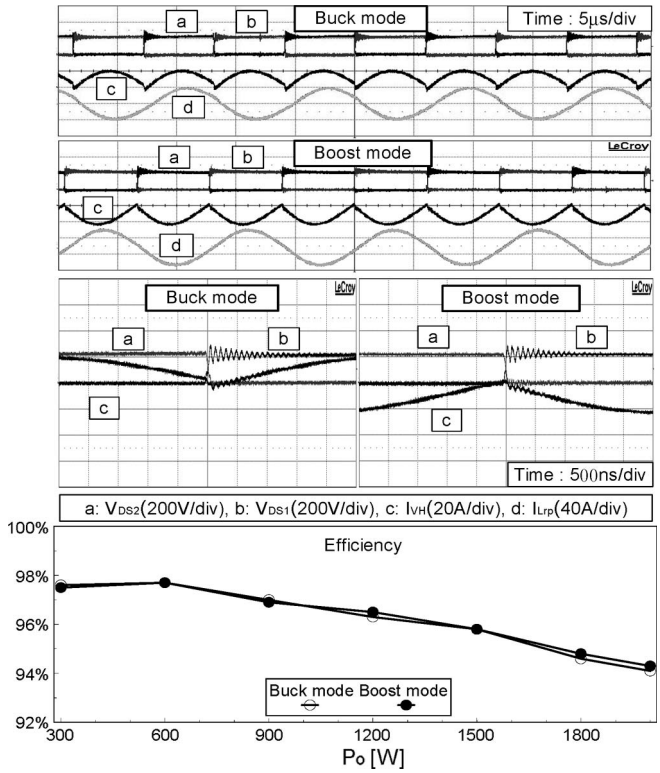

Fig. 5. Measured waveforms and efficiency plots under $P_o = 2$ kW ($V_H = 200$ V and $V_L = 24$ V).

is the limit gain in general boost converters. Accordingly, the selection range of n becomes

$$V_{L,\max}/V_{H,\min} < n < kV_{L,\min}/V_{H,\max}. \quad (5)$$

If the calculated n does not meet this condition, some adjustment should be performed.

IV. Experimental Results

The proposed converter has been designed with 2 kW ($V_H = 200-300$ V, $V_L = 18-30$ V (24-V battery), $I_{\mathrm{VL,max}} = 83$ A) and 90-kHz switching frequency for both stages. The selected switching devices are $M_1 = M_2 =$ FCA47N60 $\times 2$ and $M_3-M_6 =$ FDP3632 $\times 3$. With D_{ripple}, the calculated n is 0.266, which meets the selection range of $n = 0.15-0.3$. The transformer is constructed with two PQ4040 ferrite cores (15 T:4 T) in parallel. Since each transformer has a primary leakage inductance of 12.1 μH, 7.4 μF is selected for C_r to make f_r equal to f_s. From the L_m selection inequality, the maximum L_m is calculated as 165 μH with $T_{\mathrm{dead}} = 200$ ns, and 150 μH is used. C_b and L_b are designed as 100 μF and 20 μH, constructed with a film capacitor and a high-flux toroidal core, respectively. The controller has been implemented with TMS320F28335. Fig. 5 shows the measured waveforms and efficiency plots under bidirectional operation. The waveforms agree well with the theoretical analysis, and ZVS is well accomplished during T_{dead}. Also, it shows that the efficiencies of buck and boost modes have similar trajectories. The measured efficiency has been recorded above 94.1%. The operational duty ratios according to V_H changes are located between 0.30 and 0.45 under the maximum charge current condition so that $I_{c,\mathrm{rms}}$ has 27%–36% of $I_{\mathrm{VL,max}}$.

V. Conclusion

A two-stage isolated/bidirectional dc/dc converter with three bridges has been proposed and analyzed. The input-to-output relationships derived through analysis have shown that the converter has a simple bidirectional control scheme. Also, methods to reduce the rms currents in the HV source and link capacitor have been suggested. To verify the performance, a 2-kW prototype converter with 90-kHz switching frequency has been implemented with design guidelines derived based on rms current reduction. The experimental results show that above 94.1% of efficiency has been obtained irrespective of the power flow direction. Therefore, it may be suitable for isolated/bidirectional converters with a high voltage gain.

References

[1] W. Jiang and B. Fahimi, "Active current sharing and source management in fuel cell battery hybrid power system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 752–761, Feb. 2010.
[2] C. S. Leu and M. H. Li, "A novel current-fed boost converter with ripple reduction for high-voltage conversion applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2018–2023, Jun. 2010.
[3] M. J. Vasallo, J. M. Andujar, C. Garcia, and J. J. Brey, "A methodology for sizing backup fuel-cell/battery hybrid power systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 1964–1975, Jun. 2010.
[4] Z. Amjadi and S. S. Williamson, "A novel control technique for a switched capacitor converter based hybrid electric vehicle energy storage system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 926–934, Mar. 2010.
[5] K. Wang, C. Y. Lin, L. Xhu, D. Qu, F. C. Lee, and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," in *Proc. PET*, 1998, pp. 47–51.
[6] J. Wang, L. Zhu, D. Qu, H. Odendaal, J. Lai, and F. C. Lee, "Design, implementation, and experimental results of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-start capability," in *Proc. Power Electron. Spec. Conf.*, 2000, pp. 1058–1063.
[7] S. J. Jang, T. W. Lee, W. C. Lee, and C. Y. Won, "Bi-directional DC–DC converter for fuel cell generation system," in *Proc. Power Electron. Spec. Conf.*, 2004, pp. 4722–4728.
[8] Y. Lembeye, V. D. Bang, G. Lefebre, and J. P. Ferrieux, "Novel half-bridge inductive dc–dc isolated converters for fuel cell applications," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 203–210, Mar. 2009.
[9] F. Z. Peng, H. Li, G. J. Su, and J. S. Lawler, "A new ZVS bidirectional dc–dc converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.
[10] J. M. Kwon, E. H. Kim, B. H. Kwon, and K. H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 826–834, Mar. 2009.

Comments on "Three-Arm AC Automatic Voltage Regulator"

Jung-Min Kwon, Kyu-Tae Kim, and Bong-Hwan Kwon

***Abstract*—Some errors in the three-arm automatic voltage regulator in the paper "Three-Arm AC Automatic Voltage Regulator" by Wu *et al.* (*IEEE Trans. Ind. Electron*, vol. 58, no. 2, pp. 567–575, Feb. 2011) are pointed out, and a technique for correcting these errors is given.**

***Index Terms*—Automatic voltage regulator (AVR), three-arm.**

The paper [1] proposes a novel three-arm automatic voltage regulator (AVR) with voltage up/down capability. Fig. 1 shows the

Manuscript received March 1, 2011; revised June 1, 2011; accepted August 5, 2011. Date of publication August 30, 2011; date of current version October 4, 2011.

J.-M. Kwon is with the Department of Electrical Engineering, Hanbat National University, Daejeon 305-719, Korea (e-mail: jmkwon@hanbat.ac.kr).
K.-T. Kim and B.-H. Kwon are with the Department of Electronic and Electrical Engineering, Pohang University of Science and Technology, Pohang 790-784, Korea (e-mail: ben.kim@postech.ac.kr; bhkwon@postech.ac.kr).

Digital Object Identifier 10.1109/TIE.2011.2166234